

In the Specification:

Please amend paragraph 0014 as follows:

The present invention provides a 8F2 folded bit line DRAM cell with regularly spaced deep trench patterns in which a line mask with equal lines and spaces are used to define the active areas and in which ~~[[the]]~~ vertical transistors may be ~~[[are]]~~ formed along only one side of the trenches or alternating between the sides of adjacent trenches using a cut mask.

Please amend paragraph 0041 as follows:

The gate polysilicon region 34 is contacted by the active word line (AWL) 4. The other word lines 5 ~~[[are]]~~ also shown in Figure 2 are connected to other memory cells (not shown), which are referred to as passing word lines (PWL). The word lines 4 and 5 include a low resistive conductor layer atop an optional barrier layer, such as a dual layer conductor formed of a first tungsten nitride (WN) or polysilicon/WN layer 40 over which is formed a tungsten or tungsten silicide (WSi) layer 42. The conductive layers are surrounded by a nitride insulating layer 44 to insulate the word lines from the bit line contacts 81 ~~[[80]]~~ (shown in Figure 6H) and from the bit line. Additionally, the gate region 34 is insulated from its adjacent regions, such as from the doped regions 38, by a spacer layer 46 and a cap layer 48. The spacer layer 46 is typically formed of an oxide layer, and the cap layer 48 is typically formed of a nitride layer, though other materials may be substituted. The passing word line 5 is insulated from the doped drain regions 38 by an array top oxide (ATO) 88.